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KONRAD RAYNES & VICTOR, LLP
Suite 210
315 S. Beverly Drive
Beverly Hills, CA 90212

| EXAMINER |
|---|
| ELMORE, REBA I |

| ART UNIT | PAPER NUMBER |
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| 2189 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| ***Office Action Summary*** | **Application No.**<br>10/747,932 | **Applicant(s)**<br>SCHMISSEUR, MARK A. | |
|---|---|---|---|
| | **Examiner**<br>Reba I. Elmore | **Art Unit**<br>2189 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

# DETAILED ACTION

1. Claims 1-50 are presented for examination.

## *DRAWINGS*

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

## *SPECIFICATION*

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The disclosure is objected to because of the following informalities:

a) acronyms must be defined at their first usage - LBA in paragraph 00019 needs to be defined.

b) 'The new data may be also be transferred' is grammatically incorrect.

Appropriate correction is required.

5. Articles mentioned in paragraphs 00039, 00041, 00046 and 00048 should be provided as they are not readily available to the examiner and would allow a more complete examination of the present application.

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6. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## *35 USC 101*

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 16-29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The 'article comprising a storage medium, the storage medium comprising machine readable instructions stored thereon' would normally be considered statutory unless the specification defines '*machine readable medium*' as including *intangible media* such as signals, carrier waves, transmissions, optical waves, transmission media or other media incapable of being touched or perceived absent the tangible medium through which they are conveyed. According to paragraph 00038 the '*machine readable medium*' is defined as including *intangible media* as specified above.

## *35 USC § 102*

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Herbert.

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11. Herbert teaches the invention (claim 1) as claimed including a method comprising:

transferring from a first non-volatile storage unit of a plurality of non-volatile storage units, to a logic engine of a storage processor having a cache memory, a first unit of data stored in a stripe across the plurality of non-volatile storage units, in a first transfer operation which bypasses the cache memory with the storage processor being a RAID controller which has a CPU and a cache memory but uses the direct memory access controller and XOR buffer for storing stripe data (e.g., see col. 8, lines 6-24);

transferring from a second non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, a second unit of data stored in the stripe, in a second transfer operation which bypasses the cache memory as using the direct memory access controller and XOR buffer for parity data and not using the cache buffer (e.g., see col. 8, lines 6-24); and,

constructing in the logic engine a third unit of data using the first unit of data transferred to the logic engine in the first transfer operation and using the second unit of data transferred to the logic engine in the second transfer operation as the parity operation (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 2, Herbert teaches transferring the constructed third unit of data to a third non-volatile storage unit of the plurality of non-volatile storage units in a third transfer operation and storing the constructed third unit of data in the stripe (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 3, Herbert teaches the third transfer operation bypasses the cache memory (e.g., see Figures 1 and 2).

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As to claim 4, Herbert teaches the plurality of non-volatile storage units are arranged in a Redundant Array of Independent Disks (RAID) organization (e.g., see Figure 1).

As to claim 5, Herbert teaches the second unit of data is parity data (e.g., see col. 5, lines 11-20).

As to claim 6, Herbert teaches each non-volatile storage unit is a disk drive (e.g., see Figure 1).

As to claim 7, Herbert teaches the stripe is organized as a RAID stripe of blocks of data including a block of parity data and each of the units of data is a block of data of the RAID stripe (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 8, Herbert teaches the logic engine includes a store queue capable of storing a block of data from the RAID stripe with the store queue being a FIFO buffer (e.g., see Figure 2).

As to claim 9, Herbert teaches the cache memory of the logic engine is a random access memory (RAM) (e.g., see col. 8, lines 14-23).

As to claim 10, Herbert teaches the constructing in the logic engine a third unit of data includes applying the first unit of data transferred to the logic engine in the first transfer operation, to a store queue of the logic engine and performing an exclusive-OR logic function operation on the contents of the first store queue and the applied first unit of data and includes applying the second unit of data transferred to the logic engine in the second transfer operation, to the store queue of the logic engine and performing an exclusive XOR logic function operation on the contents of the store queue and the applied second unit of data (e.g., see col. 7, line 63 to col. 10, line 62).

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As to claim 11, Herbert teaches transferring from a fourth non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, a fourth unit of data stored in the stripe, in a fourth transfer operation which bypasses the cache memory (e.g., see col. 7, line 63 to col. 10, line 62);

transferring from a fifth non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, a fifth unit of data stored in the stripe, in a fifth transfer operation which bypasses the cache memory (e.g., see col. 7, line 63 to col. 10, line 62); and,

wherein the constructing in the logic engine the third unit of data also uses the fourth unit of data transferred to the logic engine in the fourth transfer operation and using the fifth unit of data transferred to the logic engine in the fifth transfer operation prior to the transferring the constructed third unit of data to the third non-volatile storage unit in the third transfer operation (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 12, Herbert teaches each additional non-volatile storage unit of the plurality of storage units transferring from an additional non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, an additional unit of data stored in the stripe, in an additional transfer operation which bypasses the cache memory (e.g., see col. 7, line 63 to col. 10, line 62); and,

wherein the constructing in the logic engine the third unit of data also uses the additional unit of data transferred to the logic engine in the additional transfer operation prior to the transferring the constructed third unit of data to the third non-volatile storage unit in the third transfer operation (e.g., see col. 7, line 63 to col. 10, line 62).

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As to claim 13, Herbert teaches transferring to the logic engine, a fourth unit of data which is new data to be stored in the stripe, wherein the first unit of data is old data to be replaces by the new data in the stripe, the second unit of data is old parity data to be replaced in the stripe and wherein the constructing in the logic engine the third unit of data constructs a replacement unit of parity data using the new data transferred to the logic engine, the method further comprising transferring the third unit of new parity data to the second non-volatile storage unit to replace the second unit of old parity data (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 14, Herbert teaches transferring the constructed third unit of data to a host in a third transfer operation (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 15, Herbert teaches the storage processor issues read commands to the first and second non-volatile storage units so that the first and second units for data are accessed from the first and second non-volatile storage units at least partially in parallel as the FIFO being dual ported (e.g., see col. 8, lines 25-30).

12. Herbert teaches the invention (claim 16) as claimed including an article comprising a storage medium, the storage medium comprising machine readable instructions stored thereon to:

transfer from a first non-volatile storage unit of a plurality of non-volatile storage units, to a logic engine of a storage processor having a cache memory, a first unit of data stored in a stripe across the plurality of non-volatile storage units, in a first transfer operation which bypasses the cache memory with the storage processor being a RAID controller which has a CPU and a cache memory but uses the direct memory access controller and XOR buffer for determining parity data and storing stripe data (e.g., see col. 8, lines 6-24);

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transfer from a second non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, a second unit of data stored in the stripe, in a second transfer operation which bypasses the cache memory as using the direct memory access controller and XOR buffer for parity data and not using the cache buffer (e.g., see col. 8, lines 6-24); and

construct in the logic engine a third unit of data using the first unit of data transferred to the logic engine in the first transfer operation and using the second unit of data transferred to the logic engine in the second transfer operation as parity operations (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 17, Herbert teaches the storage medium further comprises machine readable instructions stored thereon to transfer the constructed third unit of data to a third non-volatile storage unit of the plurality of non-volatile storage units in a third transfer operation and store the constructed third unit of data in the stripe (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 18, Herbert teaches the third transfer operation bypasses the cache memory (e.g., see Figures 1 and 2).

As to claim 19, Herbert teaches the plurality of non-volatile storage units are arranged in a RAID organization (e.g., see Figure 1).

As to claim 20, Herbert teaches the second unit of data is parity data (e.g., see col. 5, lines 11-20).

As to claim 21, Herbert teaches each non-volatile storage unit is a disk drive (e.g., see Figure 1).

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As to claim 22, Herbert teaches the stripe is organized as a RAID stripe of blocks of data including a block of parity data and each of the units of data is a block of data of the RAID stripe (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 23, Herbert teaches the logic engine includes a store queue capable of storing a block of data from the RAID stripe with the store queue being a FIFO buffer (e.g., see Figure 2).

As to claim 24, Herbert teaches the cache memory of the logic engine is a random access memory (RAM) (e.g., see col. 8, lines 14-23).

As to claim 25, Herbert teaches the machine readable instructions to construct in the logic engine a third unit of data include machine readable instructions stored on the storage medium to apply the first unit of data transferred to the logic engine in the first transfer operation, to a store queue of the logic engine and perform an exclusive-OR logic function operation on the contents of the first store queue and the applied first unit of data, and to apply the second unit of data transferred to the logic engine in the second transfer operation, to the store queue of the logic engine and perform an exclusive-OR logic function operation on the contents of the store queue and the applied second unit of data (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 26, Herbert teaches the storage medium further comprises machine readable instructions stored thereon to transfer from a fourth non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, a fourth unit of data stored in the stripe, in a fourth transfer operation which bypasses the cache memory (e.g., see col. 7, line 63 to col. 10, line 62);

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transfer from a fifth non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, the fifth unit of data stored in the stripe, in a fifth transfer operation which bypasses the cache memory (e.g., see col. 7, line 63 to col. 10, line 62); and,

wherein the machine readable instructions to construct in the logic engine a third unit of data include machine readable instructions stored on the storage medium to use the fourth unit of data transferred to the logic engine in the fourth transfer operation and to use the fifth unit of data transferred to the logic engine in the fifth transfer operation prior to the transferring the constructed third unit of data to the third non-volatile storage unit in the third transfer operation (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 27, Herbert teaches the storage medium further comprises machine readable instructions stored thereon to:

transfer to the logic engine, a fourth unit of data which is new data to be stored in the stripe, wherein the first unit of data is old data to be replaced by the new data in the stripe, the second unit of data is old parity data to be replaced in the stripe and wherein the machine readable instructions to construct in the logic engine a third unit of data include machine readable instructions stored on the storage medium to construct a replacement unit of parity data using the new data transferred to the logic engine, the wherein the storage medium further comprises machine readable instructions stored thereon to transfer the third unit of new parity data to the second non-volatile storage unit to replace the second unit of old parity data (e.g., see col. 7, line 63 to col. 10, line 62).

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As to claim 28, Herbert teaches the storage medium further comprises machine readable instructions stored thereon to transfer the constructed third unit of data to a host in a third transfer operation (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 29, Herbert teaches the storage medium further comprises machine readable instructions stored thereon to issue read commands to the first and second non-volatile storage units so that the first and second units of data are accessed from the first and second non-volatile storage units at least partially in parallel as the FIFO buffer being dual ported (e.g., see col. 8, lines 25-30).

13. Herbert teaches the invention (claim 30) as claimed including a system comprising:

at least one memory which includes an operation system and an application (e.g., see Figures 1 and 2);

a processor coupled to the memory (e.g., see Figures 1 and 2);

data storage having a plurality of non-volatile storage units (e.g., see Figure 2);

a data storage processor adapted to manage Input/Output (I/O) access to the data storage and having a cache memory and a logic engine as a RAID controller (e.g., see Figure 1);

a device driver executable by the processor in the memory, wherein at least one of the application, operating system, device driver and the storage processor is adapted to (e.g., see Figure 1);

transfer from a first non-volatile storage unit to the logic engine of the storage processor, a first unit of data stored in a stripe across the plurality of non-volatile storage units, in a first transfer operation which bypasses the cache memory with the storage processor being a RAID

controller which has a CPU and a cache memory but uses the direct memory access controller and XOR buffer for storing stripe data (e.g., see col. 8, lines 6-24);

transfer from a second non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, a second unit of data stored in the stripe, in a second transfer operation which bypasses the cache memory (e.g., see col. 8, lines 6-24);

construct in the logic engine a third unit of data using the first unit of data transferred to the logic engine in the first transfer operation and using the second unit of data transferred to the logic engine in the second transfer operation as the parity operation (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 31, Herbert teaches at least one of the application, operating system, device driver and the storage processor is further adapted to transfer the constructed third unit of data to a third non-volatile storage unit of the plurality of non-volatile storage units in a third transfer operation and store the constructed third unit of data in the stripe (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 32, Herbert teaches the third transfer operation bypasses the cache memory (e.g., see Figures 1 and 2).

As to claim 33, Herbert teaches the plurality of non-volatile storage units are arranged in a RAID organization (e.g., see Figure 1)

As to claim 34, Herbert teaches the second unit of data is parity data (e.g., see col. 5, lines 11-20).

As to claim 35, Herbert teaches each non-volatile storage unit is a disk drive (e.g., see Figure 1).

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As to claim 36, Herbert teaches the stripe is organized as a RAID stripe of blocks of data including a block of parity data and each of the units of data is a block of data of the RAID stripe (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 37, Herbert teaches the logic engine includes a store queue capable of storing a block of data from the RAID stripe with the store queue being a FIFO buffer (e.g., see Figure 2).

As to claim 38, Herbert teaches the cache memory of the logic engine is a random access memory (e.g., see col. 8, lines 14-23).

As to claim 39, Herbert teaches the logic engine is a third unit of data, at least one application, operating system, device driver and the storage processor is further adapted to apply the first unit of data transferred to the logic engine in the first transfer operation, to a store queue of the logic engine and perform an exclusive-OR logic function operation on the contents of the first store queue and the applied first unit of data and to apply the second unit of data transferred to the logic engine in the second transfer operation, to the store queue of the logic engine and perform an exclusive-OR logic function operation on the contents of the store queue and the applied second unit of data (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 40, Herbert teaches at least one application, operating system, device driver and the storage processor is further adapted to transfer from a fourth non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, a fourth unit of data stored in the stripe in a fourth transfer operation which bypasses the cache memory (e.g., see col. 7, line 63 to col. 10, line 62);

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transfer from a fifth non-volatile storage unit of the plurality of non-volatile storage units, to the logic engine, a fifth unit of data stored in the stripe in a fifth transfer operation which bypasses the cache memory (e.g., see col. 7, line 63 to col. 10, line 62); and,

wherein to construct in the logic engine a third unit of data, an application, operating system, device driver and the storage processor is further adapted to use the fourth unit of data transferred to the logic engine in the fourth transfer operation and to use the fifth unit of data transferred to the logic engine in the fifth transfer operation prior to the transferring the constructed third unit of data to the third non-volatile storage unit in the third transfer operation (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 41, Herbert teaches an application, operating system, device driver and the storage processor is further adapted to transfer to the logic engine, a fourth unit of data which is new data to be stored in the stripe, wherein the first unit of data is old data to be replaced by the new data in the stripe, the second unit of data is old parity data to be replaced in the stripe and wherein the machine readable instructions to construct in the logic engine a third unit of data include machine readable instructions stored on the storage medium to construct a replacement unit of parity data using the new data transferred to the logic engine and wherein the storage medium further comprises machine readable instructions stored thereon to transfer the third unit of new parity data to the second non-volatile storage unit to replace the second unit of old parity data (e.g., see col. 7, line 63 to col. 10, line 62).

As to claim 42, Herbert teaches an application, operating system, device driver and the storage processor is further adapted to transfer the constructed third unit of data to a host in a third transfer operation (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62).

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As to claim 43, Herbert teaches an application, operating system, device driver and the storage processor is further adapted to issue read commands to the first and second non-volatile storage units so that the first and second units of data are accessed from the first and second non-volatile storage units at least partially in parallel as the FIFO being dual ported (e.g., see col. 8, lines 25-30).

14. Herbert teaches the invention (claim 44) as claimed including a device for use with a data storage having a plurality of non-volatile storage units, comprising:

a data storage processor adapted to manage I/O access to the data storage and having a cache memory and a logic engine wherein the storage processor is further adapted to (e.g., see Figures 1-2);

transfer from a first non-volatile storage unit to the logic engine of the storage processor, a first unit of data stored in a stripe across the plurality of non-volatile storage units, in a first transfer operation which bypasses the cache memory (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62);

transfer from a second non-volatile storage unit of the plurality of non-volatile storage units, o the logic engine, a second unit of data stored in the stripe, in a second transfer operation which bypasses the cache memory (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62); and,

construct in the logic engine a third unit of data using the first unit of data transferred to the logic engine in the first transfer operation and using the second unit of data transferred to the logic engine in the second transfer operation (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62).

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As to claim 45, Herbert teaches the device is further adapted to transfer the constructed third unit of data to a third non-volatile storage unit of the plurality of non-volatile storage units in a third transfer operation, and store the constructed third unit of data in the stripe (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62).

As to claim 46, Herbert teaches the third transfer operation bypasses the cache memory (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62).

As to claim 47, Herbert teaches each non-volatile storage unit is a disk drive, the plurality of non-volatile storage units are arranged in a RAID organization, the stripe is organized as a RAID stripe of blocks of data including a block of parity data and each of the units of data is a block of data of the RAID stripe (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62).

As to claim 48, Herbert teaches the logic engine includes a store queue capable of storing a block of data from the RAID stripe, the cache memory of the logic engine is a random access memory and to construct in the logic engine a third unit of data, the storage processor is further adapted to apply the first unit of data transferred to the logic engine in the first transfer operation, to a store queue of the logic engine and perform an exclusive-OR logic function operation on the contents of the first store queue and the applied first unit of data and to apply the second unit of data transferred to the logic engine in the second transfer operation, to the store queue of the logic engine and perform an exclusive-OR logic function operation on the contents of the store queue and the applied second unit of data (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62).

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As to claim 49, Herbert teaches the storage processor is further adapted to transfer the constructed third unit of data to a host in a third transfer operation (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62).

As to claim 50, Herbert teaches the storage processor is further adapted to issue read commands t the first and second non-volatile storage units so that the first and second units of data are accessed from the first and second non-volatile storage units at least partially in parallel as the FIFO buffer being dual ported (e.g., see Figures 1-2 and col. 7, line 63 to col. 10, line 62).

## *CONCLUSION*

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Tuesday and Thursday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2189

Saturday, June 24, 2006

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